Agenda

- Program goals
- Processor enhancements
- Processor structures
  - Pipelines
  - Front-end
  - Functional units
  - Caches
- System bus
- Reliability features
- Summary
Program Goals

- Builds on Itanium™ processor’s EPIC design philosophy
- 100% Itanium Processor Family binary compatibility
- World class performance
  - high performance for commercial servers
  - high integer and floating-point performance
- Support for mission critical applications
  - Robust error recovery and containment
Program Goals

Architecture Philosophy

- Builds on Itanium™ processor’s EPIC features to achieve higher instruction-level parallelism
  - Prefetch/branch/cache hints, speculation, predication, register stacking = same as the Itanium processor.
  - Provide performance scaling + binary compatibility with Itanium-based applications/OSes
    - Full hardware score-board design to resolve register hazards between instruction groups

Same programming model as Itanium processor
No code changes required
McKinley Optimizations

- Improved dynamic properties
  - Target production frequency is 1 GHz
  - Reduced L1, L2, L3 latencies
  - L3 cache has been incorporated on die
  - Improved L2 cache capacity
  - Improved FSB bandwidth
  - Lower branch prediction penalties

McKinley provides significant speed ups on existing Itanium™ processor binaries
McKinley Optimizations

- Reduced execution paths
  - More parallelism/resources
    - More integer, multi-media units and memory ports
  - Short latencies
    - Fully bypassed functional units
    - Very Low L1D/L2/L3 Cache Latencies
    - Low latency FP execution
  - Many more ways to issue/execute 6 insts/clk

McKinley provides performance headroom for re-optimized binaries

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Processor Enhancements

**Micro-Architectural Enhancements**

**Itanium™ Processor**
- **System Bus**
  - 64 bits wide
  - 133MHz/266 MT/s
  - 2.1 GB/s
- **Width**
  - 2 bundles per clock
  - 4 integer units
  - 2 load or stores per clock
  - 9 issue ports
- **Caches**
  - L1 – 2X16KB - 2 clock latency
  - L2 – 96K – 12 clock latency
  - L3 - 4MB external –20 clk
  - 11.7 GB/s bandwidth
- **Addressing**
  - 44 bit physical addressing
  - 50 bit virtual addressing
  - Maximum page size of 256MB

**McKinley**
- **System Bus**
  - 128 bits wide
  - 200MHz/400 MT/s
  - 6.4 GB/s
- **Width**
  - 2 bundles per clock
  - 6 integer units
  - 2 loads and 2 stores per clock
  - 11 issue ports
- **Caches**
  - L1 – 2X16KB - 1 clock latency
  - L2 – 256K – 5 clock latency
  - L3 - 3MB – 12 clk
  - 32 GB/s bandwidth
- **Addressing**
  - 50 bit physical addressing
  - 64 bit virtual addressing
  - Maximum page size of 4GB
Processor Enhancements

Architectural Changes

– Beneficial to compilers
  – Improved data/control speculation support
    • ALAT - fully associative = minimize thrashing
    • processor directly vectors to recovery code for reduced speculation costs
  – 64-bit Long Branch Instruction

– Beneficial to OS and System designs
  – Full 64-bit virtual addressing
  – Full 2**24 virtual address spaces
  – 4GB virtual pages = reduced TLB pressure
  – 50-bit Physical addressing = very large memory/IO spaces

Changes provide more flexibility to compiler, OS and system designs
McKinley Microarchitecture

- Full Chip Block Diagram
- Pipelines
- Front-end and Branch prediction
- Functional Units
- Caches
- System Bus
McKinley Block Diagram

Processor Structure

L3 Cache

ECC

L2 Cache - Quad Port

Branch Prediction

Instruction Queue

L1 Instruction Cache and Fetch/Pre-fetch Engine

ITLB

B B B

M M M M I I F F

Register Stack Engine / Re-Mapping

11 Issue Ports

Branch & Predicate Registers

128 Integer Registers

128 FP Registers

Branch Units

Integer and MM Units

Quad-Port L1 Data Cache and DTLB

ALAT

IA-32 Decode and Control

IA-32 Decode and Control

Floating Point Units

Bus Controller

Controller

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### McKinley Pipelines

<table>
<thead>
<tr>
<th>Pipeline Stage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPG</td>
<td>IP Generate, L1I Cache (6 inst) and TLB access</td>
</tr>
<tr>
<td>ROT</td>
<td>Instruction Rotate and Buffer (6 inst)</td>
</tr>
<tr>
<td>EXP</td>
<td>Expand, Port Assignment and Routing</td>
</tr>
<tr>
<td>REN</td>
<td>Integer and FP Register Rename (6 inst)</td>
</tr>
<tr>
<td>REG</td>
<td>Integer and FP Register File read (6)</td>
</tr>
<tr>
<td>L2N-L2I-L2A-L2M-L2D-L2C-L2W</td>
<td>ALU Execute (6), L1D Cache and TLB access + L2 Cache Tag Access (4)</td>
</tr>
</tbody>
</table>

- **Short 8-stage in-order main pipeline**
  - In-order issue, out-of-order completion
  - Reduced branch misprediction penalties
  - Fully interlocked, no way-prediction or flush/replay mechanism

**Pipelines are designed for very low latency**
McKinley Issue Ports

Issue ports
- 4 Mem/ALU/Multi-Media
- 2 Integer/ALU/Multi-Media
- 2 FMAC
- 3 branch

4 memory ports
- Integer: allow 2 load AND 2 store per clk
- FP: 2 FP load pairs AND 2 store per clk to feed 2 FMACs

Substantial performance headroom for FP and integer kernels
### Processor Pipeline

**McKinley Dispersal Matrix**

<table>
<thead>
<tr>
<th></th>
<th>MII</th>
<th>MLI</th>
<th>MMI</th>
<th>MFI</th>
<th>MMF</th>
<th>MIB</th>
<th>MBB</th>
<th>BBB</th>
<th>MBB</th>
<th>MFM</th>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

* hint in first bundle

- **Green** Possible McK full issue
- **Orange** Possible Itanium™ processor and McK full issue

**McKinley allows more compiler dispersal options**
### McKinley Unit Latencies

<table>
<thead>
<tr>
<th>Producing Class Instruction</th>
<th>Consuming Class Instruction</th>
<th>Integer</th>
<th>Media</th>
<th>Load Address</th>
<th>Store Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mem/integer ports ALU</td>
<td>Integer</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Integer only ports ALU</td>
<td>Integer</td>
<td>1</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Multimedia</td>
<td></td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Integer Loads (L1D hit)</td>
<td></td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

**Short latencies and full bypasses, improve performance for re-optimized code**
### Floating Point Latencies

<table>
<thead>
<tr>
<th>Operation</th>
<th>Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>FP Load (4)</td>
<td>6</td>
</tr>
<tr>
<td>(L2 Cache hit)</td>
<td></td>
</tr>
<tr>
<td>FMAC,FMISC (2)</td>
<td>4</td>
</tr>
<tr>
<td>FP -&gt; Int (getf)</td>
<td>5</td>
</tr>
<tr>
<td>Int -&gt; FP (setf)</td>
<td>6</td>
</tr>
<tr>
<td>Fcmp to branch</td>
<td>2</td>
</tr>
<tr>
<td>Fcmp to qual pred</td>
<td>2</td>
</tr>
</tbody>
</table>

**Short latencies = performance upside for re-optimized FP code**

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Branch Prediction

- Zero clock branch prediction
  - 2 level branch prediction hierarchy
    - L1IBR – Level 1 Branch Cache
      - Part of the L1 I-cache
      - 1K trigger predictions + 0.5K target addresses
    - L2B - Level 2 Branch Cache (12K histories)
    - PHT - Pattern History Table (16K counters)

- Reduced prediction penalties
  - IP-relative branch w/correct prediction - 0 cycle
  - IP-relative branch w/wrong target - 1 cycle
  - Return branch w/correct prediction - 1 cycle
  - Last branch in counted loop prediction - 0 cycle
  - Branch Misprediction - 6 cycle

Reduced branch penalties speed up existing code
Instruction Prefetching

- **Streaming prefetching**
  - Initiated by br.many (hint on branch inst)
    - CPU prefetches ahead the sequential execution stream
    - Streaming prefetch is cancelled by:
      - a predicted-taken branch in the front-end
      - a branch misprediction occurs on the back-end
      - Software cancels the prefetch with a brp instruction

- **Branch Prefetching Hints**
  - Initiated by brp.few, brp.many or mov_to_br
    - One time prefetch for the target
    - Two hint prefetches can be initiated per cycle

Software initiated instruction prefetching improves performance by lowering instruction fetch penalties
## McKinley Caches

<table>
<thead>
<tr>
<th></th>
<th>L1I</th>
<th>L1D</th>
<th>L2</th>
<th>L3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>16K</td>
<td>16K</td>
<td>256K</td>
<td>3M on die</td>
</tr>
<tr>
<td><strong>Line Size</strong></td>
<td>64B</td>
<td>64B</td>
<td>128B</td>
<td>128B</td>
</tr>
<tr>
<td><strong>Ways</strong></td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td><strong>Replacement</strong></td>
<td>LRU</td>
<td>NRU</td>
<td>NRU</td>
<td>NRU</td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td>I-Fetch:1</td>
<td>INT:1</td>
<td>INT: 5</td>
<td>12</td>
</tr>
<tr>
<td><strong>(load to use)</strong></td>
<td></td>
<td>FP: NA</td>
<td>FP: 6</td>
<td></td>
</tr>
<tr>
<td><strong>Write Policy</strong></td>
<td>-</td>
<td>WT (RA)</td>
<td>WB (WA + RA)</td>
<td>WB (WA)</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>R: 32 GBs</td>
<td>R: 16 GBs</td>
<td>R: 32 GBs</td>
<td>R: 32 GBs</td>
</tr>
</tbody>
</table>

### All caches are physically indexed, pipelined, and non-blocking:

score boarded registers allow continued execution until load use

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Processor Caches

**L1D (1 clock Integer Cache)**

- High Performance 16GBs, 2 ld AND 2 st ports
  - Write Through – all stores are pushed to the L2
  - FP loads force miss, FP stores invalidate
  - True dual-ported read access – no load conflicts
  - pseudo-dual store port write access
    - 2 store coalescing buffers/port hold data until L1D update
- Store to load forwarding

One clock data cache provides a significant performance benefit
Processor Caches

L2 and L3 Cache

- **L2 256KB, 32GBs, 5 clk**
  - Data array is pseudo-4 ported - 16 banks of 16KB each

- **Non-blocking/out-of-order**
  - L2 queue (32 entries) - holds all in-flight load/stores
  - out-of-order service - smoothes over load/store/bank conflicts, fills
  - Can issue/retire 4 stores/loads per clock
  - Can bypass L2 queue (5, 7, 9 clk bypass) if
    - no address or bank conflicts in same issue group
    - no prior ops in L2 queue want access to L2 data arrays

- **Large L3 3MB, 32GBs, 12 clk cache on die!!**
  - Single ported – full cache line transfers

Large on die L2 and L3 cache provides significant performance potential
2-level TLB hierarchy

- **DTC/ITC** (32/32 entry, fully associative, .5 clk)
  - Small fast translation caches tied to L1D/L1I
    - Key to achieving very fast 1-clk L1D, L1I cache accesses

- **DTLB/ITLB** (128/128 entry, fully associative, 1 clk)
  - All architected page sizes (4K to 4GB)
  - Supports up to 64/64 ITR/DTRs
  - TLB miss starts hardware page walker

Small fast TLBs enable low latency caches
System Bus Enhancements

- Extension of the Itanium™ processor bus
  - Same protocol with minor extensions
  - Increased to 6.4GBs bandwidth
    - frequency 200MHz, 400MHz data, 128-bit data bus
  - Bus is non-blocking and out of order
    - Most transactions can be deferred for later service
    - Buffering
      - 18 bus requests/CPU are allowed to be outstanding
      - 16 Read Line + 6 Write Line + two 128 byte WC buffers

McKinley significantly extends the system bus performance level
McKinley provides several new bus transactions to improve performance/reliability

System Bus

New Bus Transactions

– **L3 cast-outs** (Normally silent L3 replacement (E->I, S->I))
  – Reduces snoop traffic in Directory based systems
  – Backward inquiry for L2, L1 coherency

– **Memory read current**
  – non-destructive (non-coherent) snoop of CPU lines
  – Used in high bandwidth graphic based systems

– **Cache Cleanse** – writes all modified lines to memory
  – M->E, Used in fault tolerant systems – invoked via PAL
Reliability Features

Error Features

- Error detection on all major arrays
  - Parity coverage on L1D, L1I, and TLBs
  - ECC on L2 and L3
    - double bit detection single bit correction - Out of path repair
    - all errors are fully contained
  - Bus is covered with parity/ECC
    - double bit detection single bit correction on transmission

- Error Isolation (end-to-end error detection)
  - From memory: unique FSB 2xECC syndrome encoding can tolerant additional single bit errors in transmission
  - Error not reported until referenced by a consuming process

McKinley provides extensive error detection/correction/containment
Reliability Features

Thermal Management

- Programmable fail-safe thermal trip
  - McKinley will reduce power consumption
    - Reduce power consumption to ~60% of peak
    - Execution rate dropped to 1 inst per clock
    - Correct Machine Check notification posted to OS
    - Full speed execution resumes when temperature drops
  - never invoked in properly designed and operating cooling systems
    - even on worse case power code

McKinley provides a thermal fail-safe mechanism in the event of a cooling failure
Summary

- McKinley builds on and extends the Itanium processor family to meet the needs of the most demanding enterprise and technical computing environments
  - Enhanced McKinley features are a result of extensible Itanium™ architecture
  - McKinley is compatible with Itanium™ processor software

- Major enhancements include:
  - Increased frequency
  - Enhanced micro-architecture – more execution units, issue ports
  - Efficient data handling; higher bandwidth and reduced latencies

- Intel estimates McKinley based systems will deliver ~1.5X – 2X performance improvement over today’s Itanium™ based systems
Micro-Architecture Comparison

Sun UltraSparc® III
- 2.4 GB/s
- 96K L1*
- 14
- 96 Registers
- 1234
- 2 Integer, 1 Branch
- 2 FP/VIS, 1 Load/Store
- 900 MHz
- 4 instructions / Cycle
- RISC Architecture

McKinley
- 6.4 GB/s
- L3 = 3 MB, L2 = 256K; L1 = 16K + 16K
- 328 Registers
- 123456789101
- 6 Integer, 3 Branch
- 2 FP, 1 SIMD
- 2 Load, 2 Store
- 1 GHz
- 6 Instructions / Cycle
- EPIC Architecture

System Bus Bandwidth
- On-die Cache
- Issue Ports
- Execution Units
- Core Frequency
- Instructions / Clk

Source: www.sun.com, The SPARC Architecture Manual (Prentice Hall)
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